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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,815	12/22/2000	Jean-Didier Allegrucci	3242P008	8894

7590 01/29/2004

Jeffrey S. Smith
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER

PEUGH, BRIAN R

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 01/29/2004

14

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/746,815

Applicant(s)

ALLEGRUCCI ET AL.

Examiner

Brian R. Peugh

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed December 11, 2003 in response to PTO Office Action dated December 3, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-15 have been presented for examination in this application. In response to the last Office Action, claims 1, 6, and 11 have been amended.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "the external alias" in lines 4 and 5. There is insufficient antecedent basis for this limitation in the claim. An "external alias" had not been previously recited.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5-8, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Virajpet et al. (US# 6,480,948) in view of James, Jr. et al. (US# 6,240,519) and Tai et al. (6,567,093). Claim 5 has been rejected according to the best possible interpretation in light of the 35 U.S.C. 122, second paragraph rejection.

Regarding claims 1, 6, and 11, Virajpet et al. teaches a system for memory aliasing system. The **processor** is able to read from an internal **ROM (memory)(31) for initialization (configuration) or boot code processing** (col. 3, lines 1-16; col. 4, lines 5-23). Section (31) of the memory map is configurable, and during a first time period, the **configurable section is aliased** so that when the processor attempts to access this section (internal ROM), the access is directed toward the external ROM (20) under control of the bus/memory controller. Thus, when the processor seeks to address 00000000h, the access is directed toward an external non-volatile memory.

A first difference between the claimed subject matter and that of Virajpet et al., disclosed supra, is that the claim recites searching for a **valid secondary initialization routine**. James, Jr. et al. teaches a system for recovering from a corrupted boot ROM image. The ROM image is found within the ROM device, and once the processor

determines that the image is corrupt, the processor continues to execute the boot block code of the ROM (col. 7, lines 54-58; col. 8, lines 4-12; Fig. 6A-6D). James, Jr. et al. teaches **searching for a secondary init. routine** in the form of determining if a floppy disk (external memory) is present in the floppy drive. If the diskette is present, the boot sequence is **initialized from the floppy disk (secondary init. routine)** without the aid of the original ROM (col. 8, line 53 – col. 9, line 1). **Bootting of the original ROM was disabled** in order for the diskette boot sequence to occur.

Another difference between the claimed subject matter and that of Virajpet et al. and James, Jr. et al., is that the claims recite that the aliasing is done for a configurable system-on-chip system, as well as that the external memory is a **flash** memory. Tai et al. teaches that the **system-on-chip** has a **configuration** including a **processor (CPU)** (2112P), **internal busses** (2113,2114), and programmable logic in the form of a **EEPROM** (electrically erasable programmable read-only-memory)(**flash**) (**programmable logic**) (col. 1, lines 45-60; col.4, lines 44-46; col. 5, lines 16-30).

Specifically regarding claim 5, the above recitations have combined to disclose that the **ROM has been programmed with an alias** (Virajpet et al.) and that a **secondary alias** (initialization scheme) was used according to a **priority** when the original was found to be corrupt (James, Jr. et al.).

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Virajpet et al., James, Jr. et al., and Tai et al. before him at the time the invention was made to modify the aliasing system of Virajpet et al. to include the recoverable ROM system of James, Jr. et al. and the system-on-chip design of Tai et

al., because then a single integrated circuit chip would yield advantages of cost reduction, easier design, and simpler mass production, as taught by Tai et al. (col. 1, lines 45-48), as well as teach a system for reflashing a corrupted ROM for future use, as taught by James, Jr. et al.

Regarding claims 2, 7, and 12, Virajpet et al. teaches **loading initialization operations** from an external non-volatile memory (**flash**) (col. 4, lines 9-13).

Regarding claim 3, 8, and 13, the changing of aliases as taught by Virajpet et al. is done during a first time period following **processor reset**, such that the processor must re-initialize from the external memory (col. 3, lines 8-13).

Claims 4, 9, 10, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Virajpet et al. (US# 6,480,948), James, Jr. et al. (US# 6,240,519) and Tai et al. (6,567,093) as applied to claims above, and further in view of Bartoli et al. (US# 6,401,164).

The difference between the claimed subject matter of claims 4, 9, and 14 and that of Virajpet et al. James, Jr. et al., and Tai et al., disclosed supra, is that the claims recite that code is executed in a manner starting from the bottom of the ROM memory. Bartoli et al. teaches both **top and bottom boot sector configurations** for an internal ROM device (Figures 1A & 1B; col. 1, line 49 – col. 2, line 19). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Virajpet et al., James Jr., et al., Tai et al., and Bartoli et al. before him at the time the invention was

made to modify the internal memory of Virajpet et al. , James Jr. et al., and Tai et al. to include reading initialization code from the top or bottom of the memory, because then greater functionality for specific system designs could be incorporated that would take advantage of reading from either the top or bottom of the internal memory for initialization routines.

Regarding claims 10 and 15, Virajpet et al. teaches a **continuing (application) program** for the initialization program setup. As seen in Figure 3, should the select signal be set, the **internal memory** ROM is directed to return requested data (col. 5, lines 12-16).

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

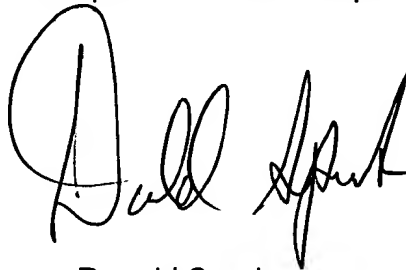
In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.



Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

DS/BRP 

January 15, 2004